In our simulation, we instantiated ALU with our input wires X, Y, Z, and our output wires Z, equal, overflow and zero.

We initialized the inputs. Firstly, we tested op\_code ALU\_OP\_AND. For test cases we tested edge cases like all 1’s and all 0’s as well as mixtures of 0’s and 1’s, and we did combinations of these. We repeated these test cases for OR, XOR and NOR.

For ADD, we made some different test cases. We chose our test cases differently to confirm that simple additions like 1+ 1, 2 + 2 work. We then chose some random intermediate cases. Lastly we chose some cases where we expected overflow to occur to confirm that our overflow output was working correctly; for instance we added 1 to the number with 1 in all 32 bits.